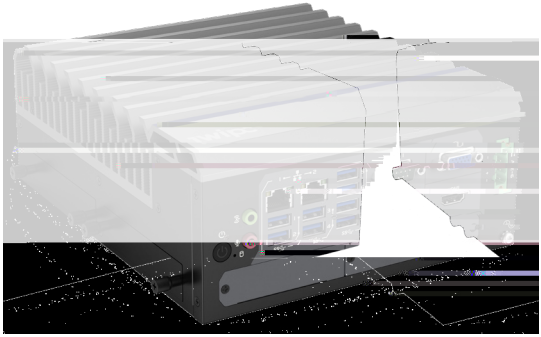
JMC-7110



Version 1.0

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1

1.1

JMC-7110 I/O
LAN, COM, DP/HDMI,
, PCIe PCI

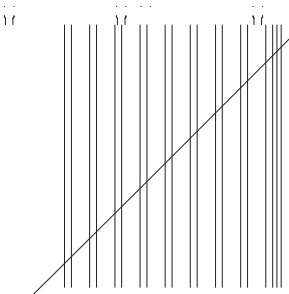
JMC-7111	1	1 x PCIex16
JMC-7112	2	2 x PCI/1 x PCIex16+1 x PCI/1 x PCIex16+1 x PCIex4
JMC-7113	3	1 x PCIex16+2 x PCI
JMC-7114	4	1 x PCIex16+2 x PCI+1 x PCIex4

1.2

	- JMC-7110	- JMC-7111	- JMC-7112	- JMC-7113	- JMC-7114
CPU	- LGA1151 Gen 6th/7th/8th/9th Core™i3/i5/i7Pentium®/Celeron®Processor				
	- Q170/H110(JMC-7114 Q170)				
	- 2x 260-Pin DDR4 SODIMM, DDR4 2133/2400 MHz 32GB ECC				
	- , HDMI 2nd/DP/DVI - 1xVGA, VGA 1920*1200@60Hz - 1xHDMI,HDMI 4096*2160@24Hz				
	- 1 x 2.5 " HDD/SSD(2) Q170 SATA RAID 0/1, - 1 x mSATA				
	- Line-out, Mic-in				
	- 2 , LAN1: I219LM, LAN2: I210AT				
USB	- Q170: 8x USB3.0, 2x USB2.0(Internal), 1x USB dongle - H110: 4x USB3.0, 4x USB2.0, 1x USB2.0(Internal)				
	- 6 COM, 2x RS232(4)/422/485 ( ), 2 x RS232/422/485+2 x RS-232 ( )				
PS2	- 1 (, PS/2 KB/Mouse)				
TPM	-				
	- 1				
	- 1x Power LED, 1x HDD LED				
	- DC IN 9~36V				

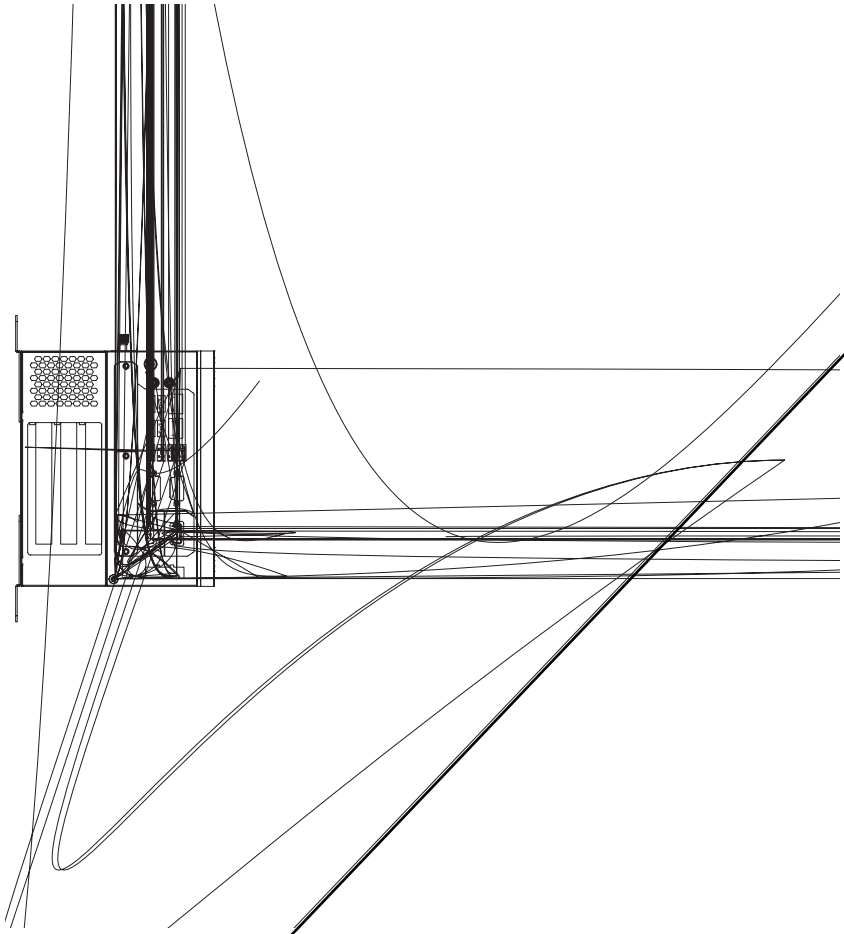
3.3 JMC-7111

mm



3.5 JMC-7113

mm



4

4.1

⚠

⚠

⚠

I/O USB I/O

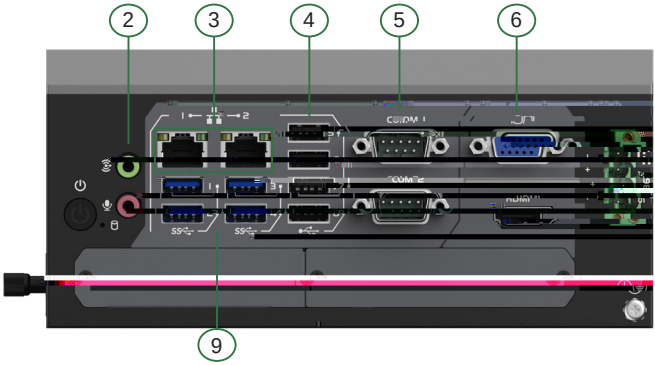
4.2

DCIN	

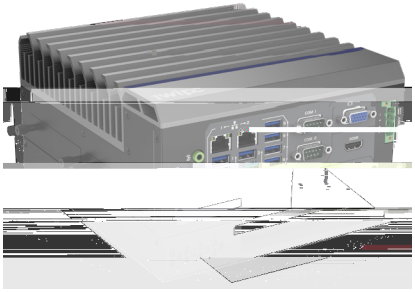
⚠

5

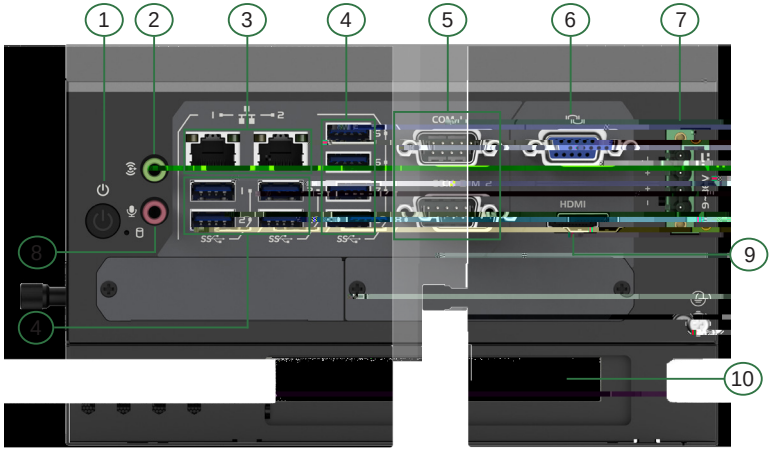
5.1.2 JMC-7110H IO



5.2 JMC-7111

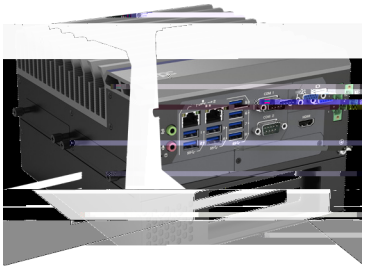


5.2.1 JMC-7111Q IO

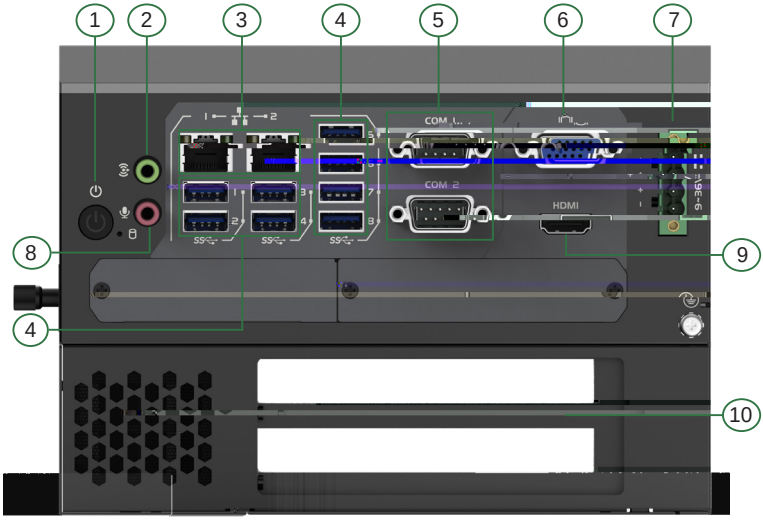


1.Power Button
2. Line out
3. LAN RJ45
4. USB3.0 USB3.0
5. COM COM
6. VGA VGA
7. DC_IN DC
8. Mic in
9. HDMI HDMI
10. JMC-7111 1 x PCIex16

5.3 JMC-7112

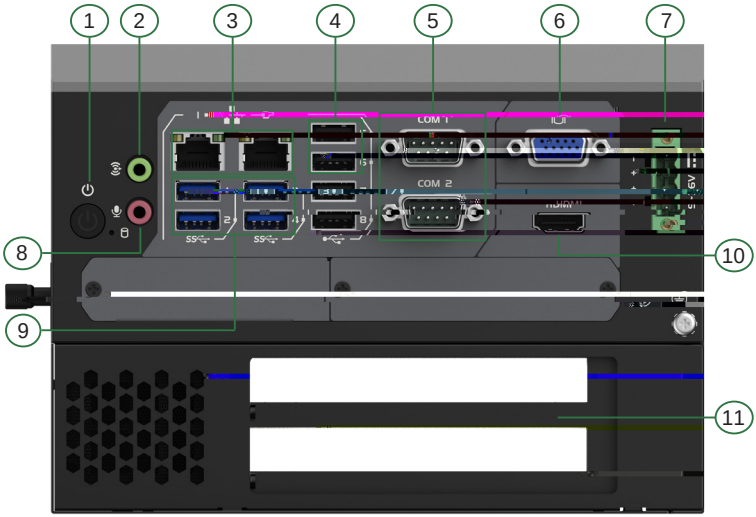


5.3.1 JMC-7112Q IO



1.Power Button
2. Line out
3. LAN RJ45
4. USB3.0 USB3.0
5. COM COM
6. VGA VGA
7. DC_IN DC
8. Mic in
9. HDMI HDMI
10. JMC-7112 2 x PCI/1PCIex16+1 x PCI/1PCIex16+1 x PCIex4

5.3.2 JMC-7112H IO

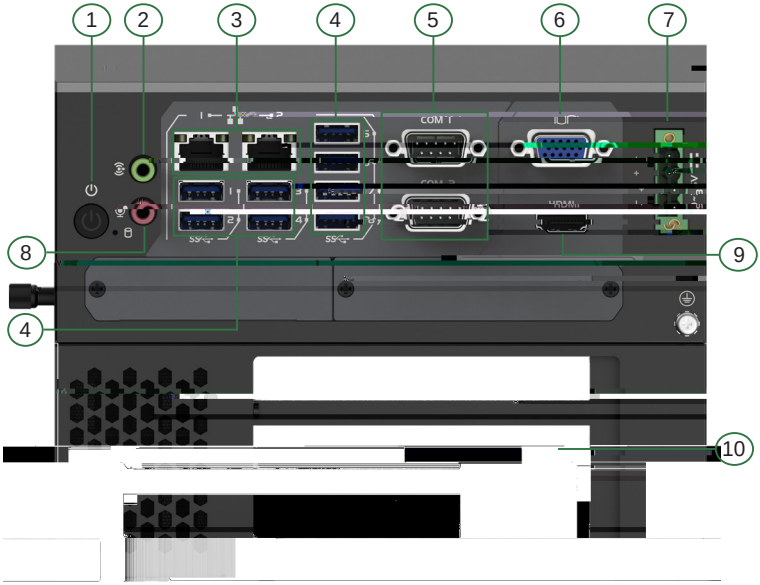


1.Power Button
2. Line out
3. LAN RJ45
4. USB2.0 USB2.0
5. COM COM
6. VGA VGA
7. DC_IN DC
8. Mic in
9. USB3.0 USB3.0
10. HDMI HDMI
11. JMC-7112 2 x PCI/1PCIex16+1 x PCI/1PCIex16+1 x PCIex4

5.4 JMC-7113

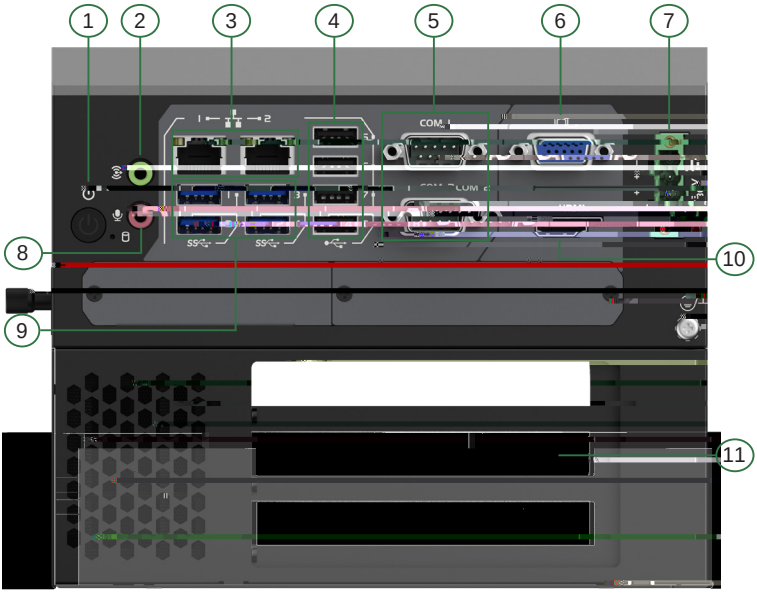


5.4.1 JMC-7113Q IO



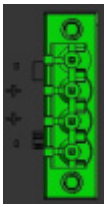
1.Power Button
2. Line out
3. LAN RJ45
4. USB3.0 USB3.0
5. COM COM
6. VGA VGA
7. DC_IN DC
8. Mic in
9. HDMI HDMI
10. JMC-7113 1 x PCIex16+2 x PCI

5.4.2 JMC-7113H IO



1.Power Button
2. Line out
3. LAN RJ45
4. USB2.0 USB2.0
5. COM COM
6. VGA VGA
7. DC_IN DC
8. Mic in
9. USB3.0 USB3.0
10. HDMI HDMI
11. JMC-7113 1 x PCIex16+2 x PCI

5.6



1	GND
2	DCIN
3	DCIN
4	GND

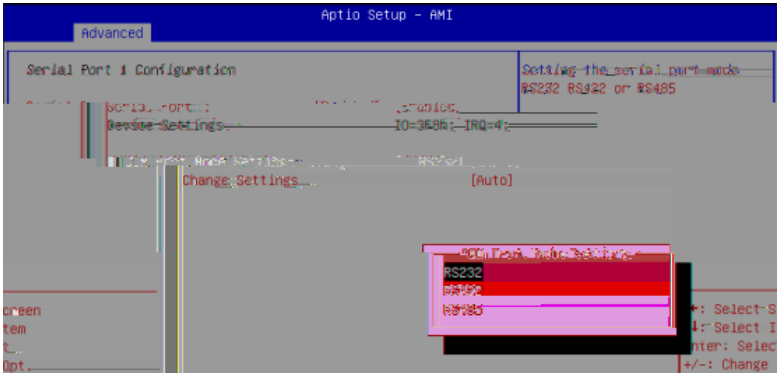
4pin 3.5mm

5.7 COM1/2



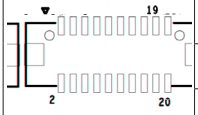
PIN	RS232	RS422	RS485
1	/	422TX-	485-
2	SIN	422TX+	485+
3	SOUT	422RX+	/
4	/	422RX-	/
5	GND	/	/
6	/	/	/
7	RTS	/	/
8	CTS	/	/
9	/	/	/

COM1/2 RS232/422/485 BIOS



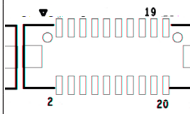
5.8

5.8.1 JDP1



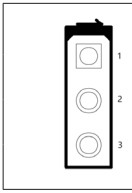
1	DP1_PWR	2	DP1_PWR
3	GND	4	GND
5	DDI2_TX0_DP	6	DDI2_TX2_DP
7	DDI2_TX0_DN	8	DDI2_TX2_DN
9	GND	10	GND
11	DDI2_TX1_DP	12	DDI2_TX3_DP
13	DDI2_TX1_DN	14	DDI2_TX3_DN
15	GND	16	DP1_CONFIG1
17	DDI2_AUXP	18	DP1_CONFIG2
19	DDI2_AUXN	20	DP1_HPD

5.8.2 JDP2



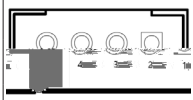
1	DP2_PWR	2	DP2_PWR
3	GND	4	GND
5	DDI3_TX0_DP	6	DDI3_TX2_DP
7	DDI3_TX0_DN	8	DDI3_TX2_DN
9	GND	10	GND
11	DDI3_TX1_DP	12	DDI3_TX3_DP
13	DDI3_TX1_DN	14	DDI3_TX3_DN
15	GND	16	DP2_CONFIG1
17	DDI3_AUXP	18	DP2_CONFIG2
19	DDI3_AUXN	20	DP2_HPD

5.8.3 CLR_CMOS1



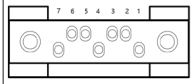
1	NC
2	PCH_RTCRST_N
3	GND

5.8.4 SATA0/1_POWER



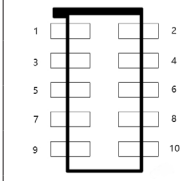
1	+V5
2	GND
3	+V12
4	GND

5.8.5 SATA0/1/2/5



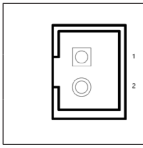
1	GND
2	SATA_TX_P
3	SATA_TX_N
4	GND
5	SATA_RX_N
6	SATA_RX_P
7	GND

5.8.6 GPIO0



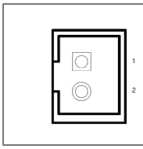
1	GPIO0_0	2	GPIO0_4
3	GPIO0_1	4	GPIO0_5
5	GPIO0_2	6	GPIO0_6
7	GPIO0_3	8	GPIO0_7
9	+5V	10	GND

5.8.14 JBUT1



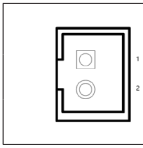
1	PWR_BUT
2	GND

5.8.15 RST_BUT1



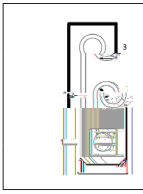
1	RESET_BUT
2	GND

5.8.16 5VPWR



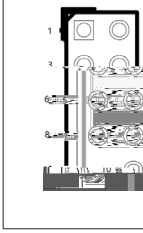
1	+V5
2	GND

5.8.17 PSON1



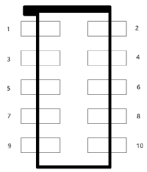
1	VCCAT
2	+V3.3SB
3	VCCATX

5.8.18 USB2H1



1	+V5	2	+V5
3	USB2_N11	4	USB2_N10
5	USB2_P11	6	USB2_P10
7	GND	8	GND
		10	GND

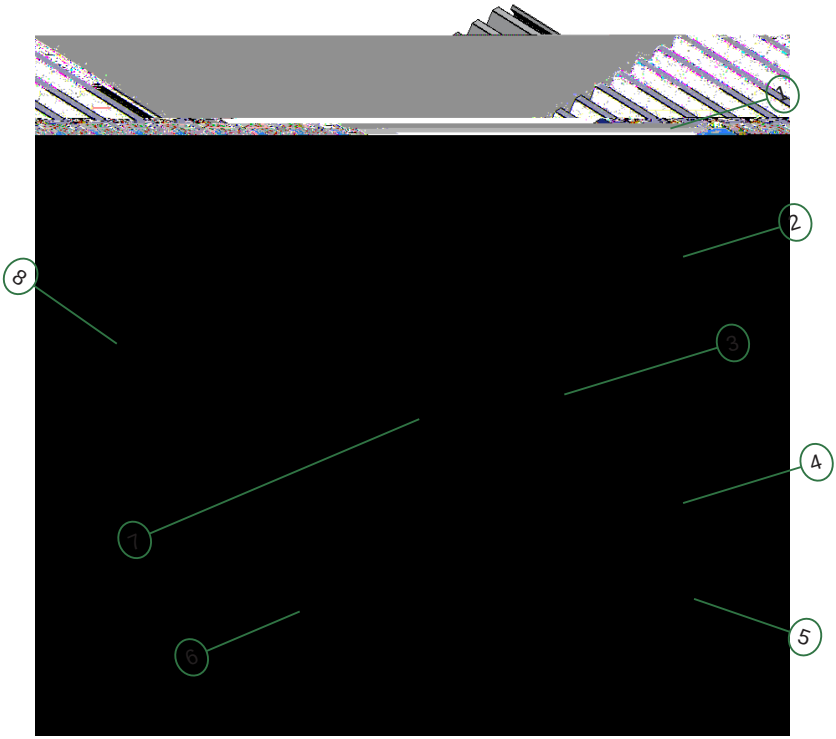
5.8.19 JSPI1



1	+V3.3	2	+V3.3
3	SPI_MISO	4	SPI_MOSI
5	SPI_CS	6	SPI_CLK
7	GND	8	SPI_WP
9	SPI_HOLD	10	NC

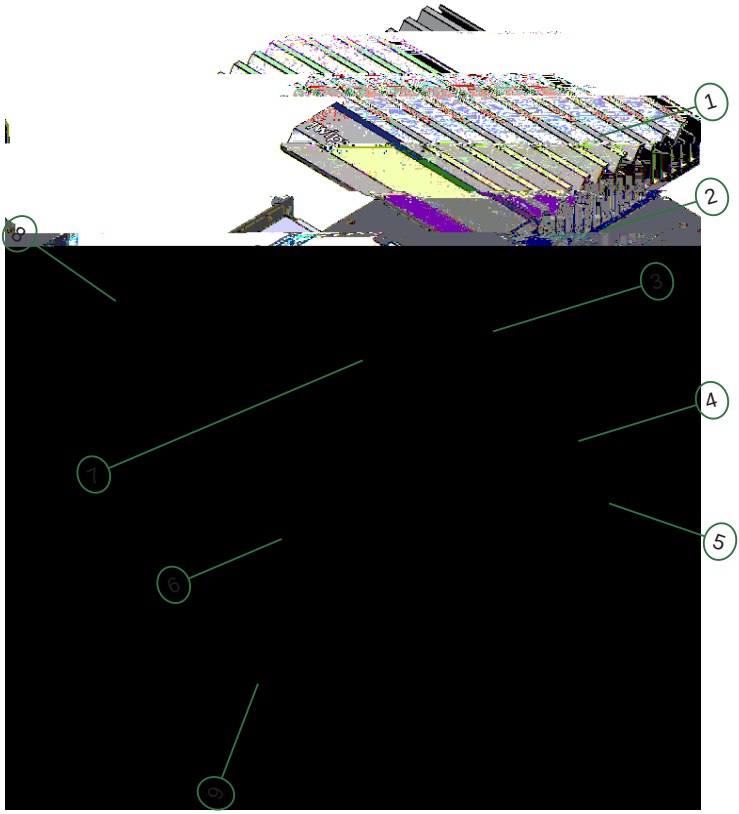
6

6.1 JMC-7110

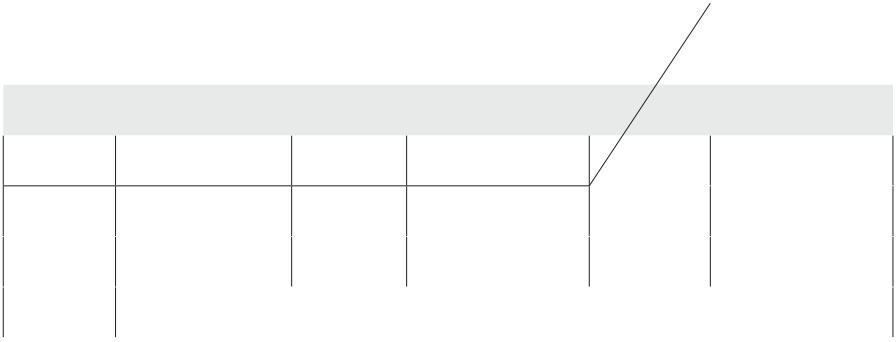


1		2		3	CPU
4		5		6	
7		8	SATA		

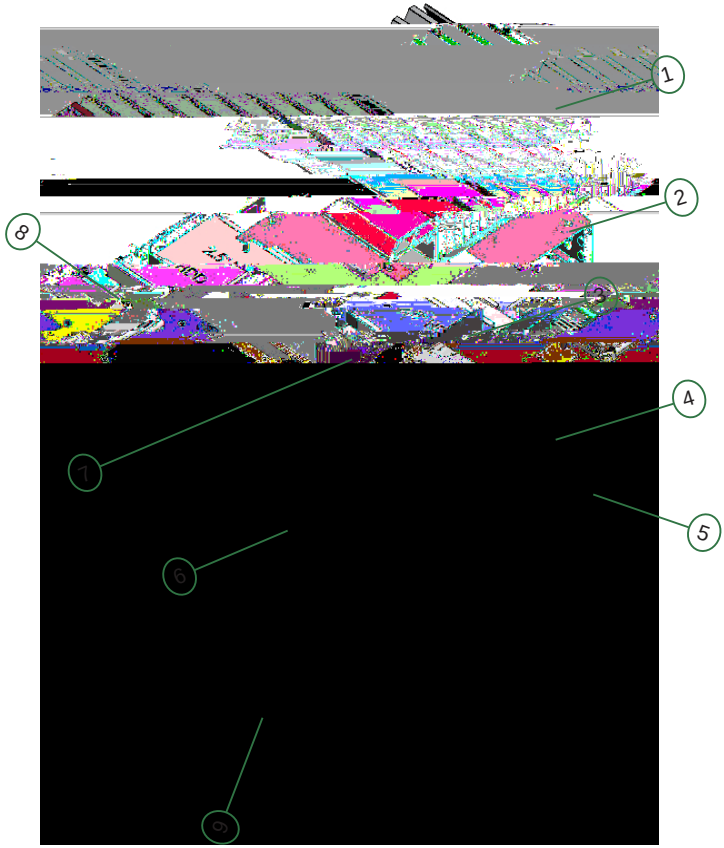
6.2 JMC-7111



1		2		3	CPU
4		5		6	
7		8	SATA		
9	(1 x PCIex16)				

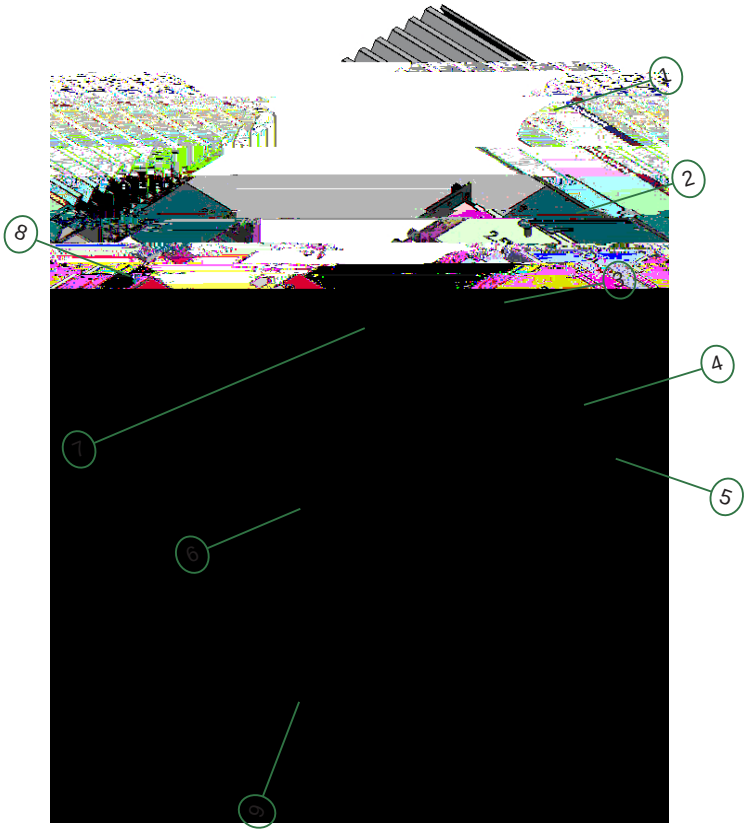


6.4 JMC-7113



1		2		3	CPU
4		5		6	
7		8	SATA		
9	(1 x PCIex16+2 x PCI)				

6.5 JMC-7114



1		2		3	CPU
4		5		6	
7		8	SATA		
9	(1 x PCIex16+2 x PCI+1 x PCIex4)				

7 BIOS

7.1 BIOS

AMI BIOS BIOS Basic Input Output System (
ROM Read-Only Memory) BIOS

a. POST(Power On Self Test)
b.
c.
d. SETUP
BIOS CMOS RAM
BIOS CMOS
BIOS

7.2 BIOS

BIOS Setup BIOS

SETUP
a. SETUP
b.

BIOS BIOS

7.2.1 BIOS

<DEL> BIOS

Press <Delete> to enter SETUP

Press <F11> to enter Boot Menu

7.2.2

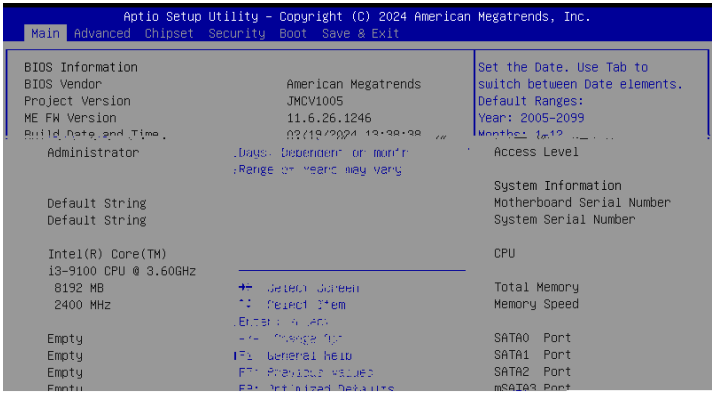
<Enter> <F1> <Esc>

← / →	
↑ / ↓	
+/ -	/
<Enter>	
<ESC>	CMOS SETUP
<F1>	
<F7>	
<F9>	
<F10>	CMOS

7.3 BIOS

Main		BIOS
Advanced		BIOS
Chipset		
Security		
Boot		
Save & Exit		BIOS

7.4 Main



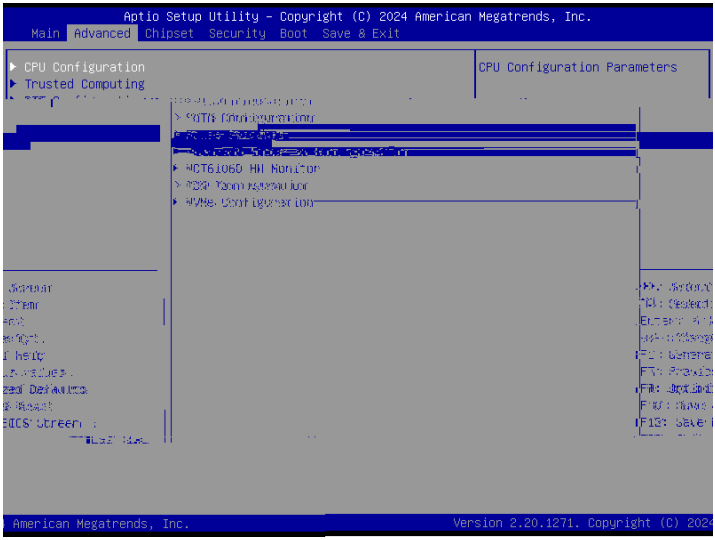
System Date ( )

, “ , / / ”

System Time

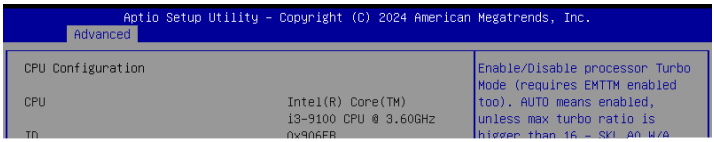
< >< >< >

7.5 Advanced



CPU Configuration	CPU	
Trusted Computing		
PTT Configuration	PTT	
SATA Configuration	SATA	
Power Configuration		
NCT6106D Super IO Configuration	Super IO	
NCT6106D HW Monitor		
CSM Configuration	CSM	
NVMe Configuration	NVMe	

CPU Configuration <Enter>

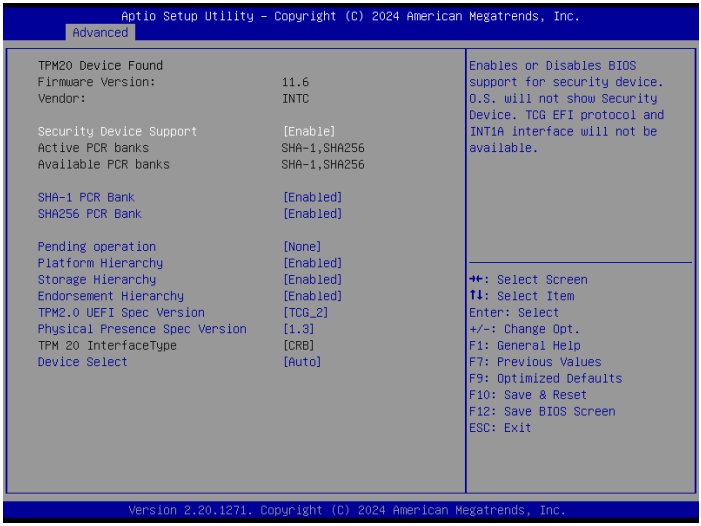


Turbo Mode

Turbo

Enabled,Disabled.

Trusted Configuration <Enter>



Security Device Support

BIOS

Disable,Enable.

- SHA-1 PCR Bank

  SHA-1 PCR Bank

  Enabled,Disabled.
- SHA256 PCR Bank

  SHA256 PCR Bank

  Enabled,Disabled.
- Pending operation

  None,TPM Clear.
- Platform Hierarchy

  Enabled,Disabled.
- Storage Hierarchy

  Enabled,Disabled.
- Endorsement Hierarchy

  Enabled,Disabled.
- TPM 2.0 UEFI Spec Vesion

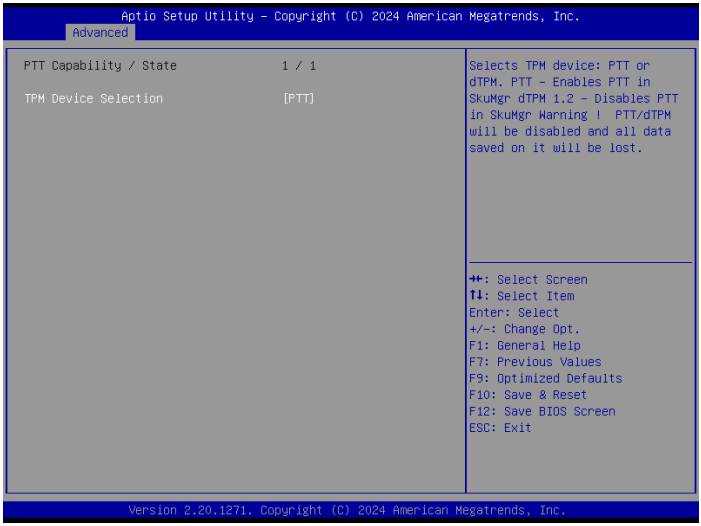
  UEFI TPM 2.0

  TCG_1_2,TCG_2.
- Physical Presence Spec Version

  1.2,1.3.
- Device Select

  TPM 1.2,TPM 2.0,Auto.

PTT Configuration <Enter>

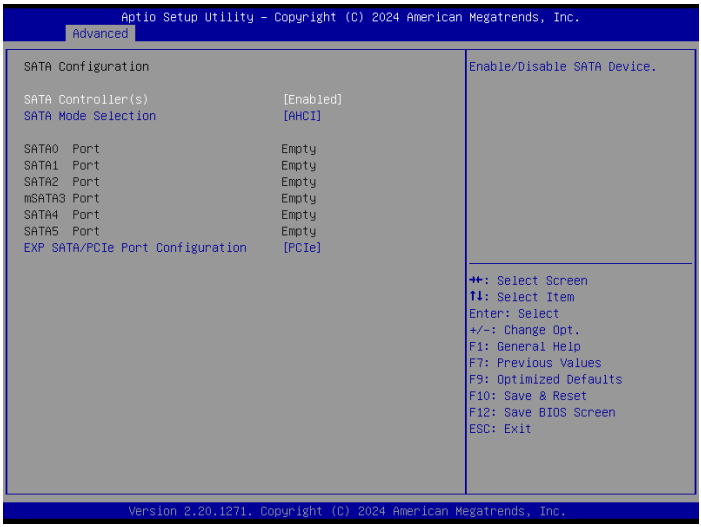


- TPM Device Selection

  TPM

  dTPM, PTT.

SATA Configuration <Enter>

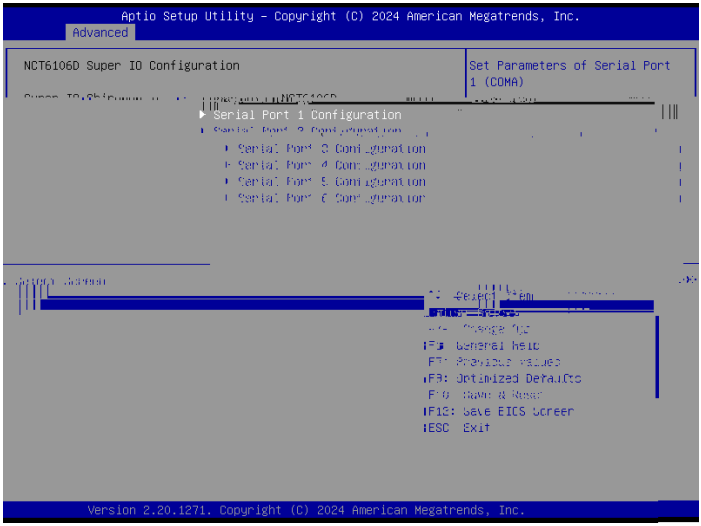


- SATA Controller

  SATA

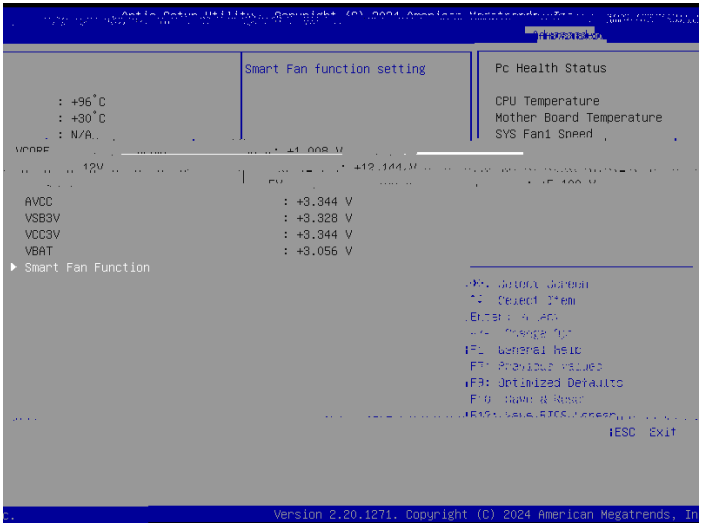
  Enabled,Disabled.

NCT6106D Super IO Configuration <Enter>



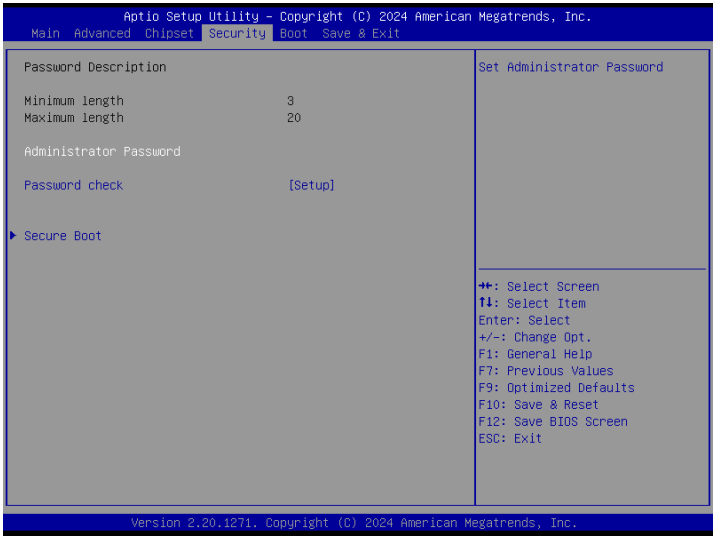
Serial Port 1/2/3/4/5/6 Configuration

NCT6106D HM Monitor <Enter>



- Smart Fan Function

7.7 Security

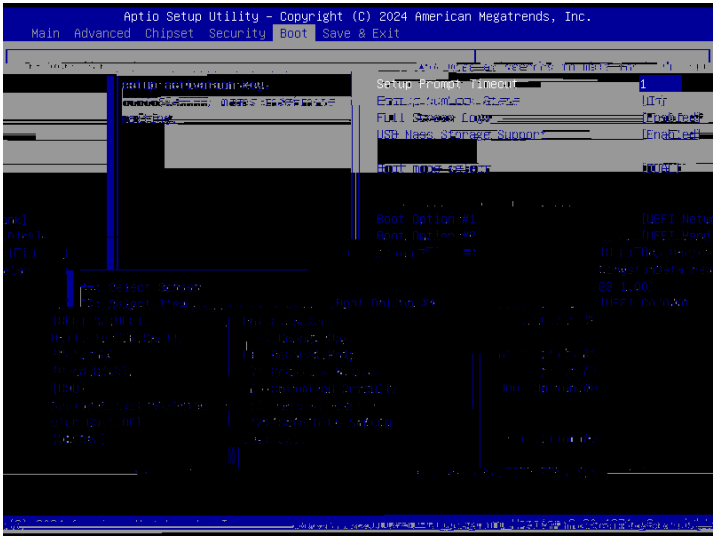


Administrator Password

1. Administrator Password <Enter>
2. “ Create New Password ” 3~20 <Enter> “ Confrm Password ” “ Invalid Password! ”

m l Inconsistent Password ” “ Enter> d M assword d ç n n N D φ g

7.8 Boot



- Setup Prompt Timeout

- Bootup NumLock State

  Numlock On NumLock

  Of Numlock

  On,Of.

  Full Screen Logo

  Logo

  Disable,Enable.

  USB Mass Storage Driver Support

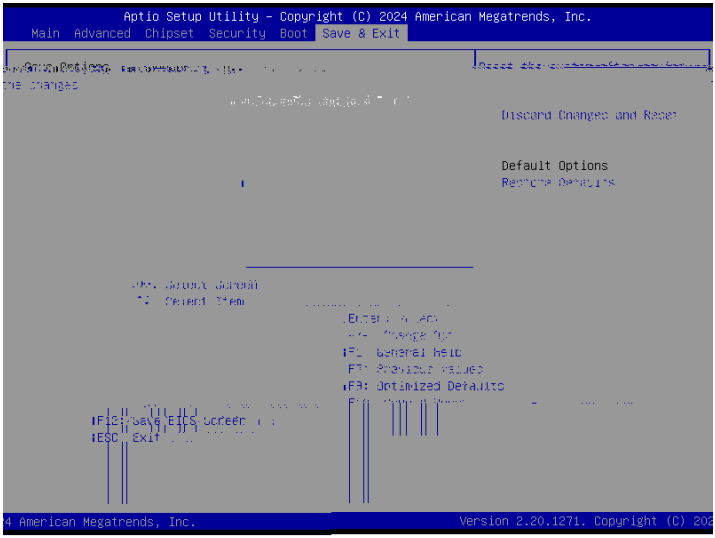
  USB

  Disable,Enable.

  Boot Option #1-9

  NVME,Hard Disk,USB Hard Disk,USB key,USB CD/DVD,Network,UEFI AP: Built-in EFI Shell.

7.9 Save&Exit



Save Changes and Reset

Discard Changes and Reset

Restore Defaults

8

JMC-7110 GPIO

8.1 GPIO

JMC-7110 GPIO
1 GPIO0 GP30/31/32/33/34/35/36/37 /
2 GPIO1 GP40/41/42/43/44/45/46/47 /
3 GPIO Group GP3x/4x Logical Device 7
4 GP3x(30~37) / Logical Device 7 CR 0xEC Bit0~Bit7 0: Output Pin / 1:Input Pin
GP4x(40~47) / Logical Device 7 CR 0xF0 Bit0~Bit7 0: Output Pin / 1:Input Pin
GP3x(30~37) Logical Device 7 CR 0xED Bit0~Bit7
GP4x(40~47) Logical Device 7 CR 0xF1 Bit0~Bit7
5 GPIO Group3 GPIO Group4 GPIO_GROUP_3_IO_REGISTER/GPIO_GROUP_3_DATA_REGISTER GPIO Group4 0x30/0x37 0x40/0x47

```
#define SuperIo_Index_Port 0x2E
#define SuperIo_Data_Port 0x2F
#define GPIO_LDN7_DEVICE 0x07
#define GPIO_GROUP_3_IO_REGISTER 0xEC
#define GPIO_GROUP_4_IO_REGISTER 0xF0
#define GPIO_GROUP_3_DATA_REGISTER 0xED
#define GPIO_GROUP_4_DATA_REGISTER 0xF1
```

GPIO Group 3

```
//a. Super IO Configuration Mode
IoWrite8(SuperIo_Index_Port, 0x87);
IoWrite8(SuperIo_Index_Port, 0x87);

//b. GPIO, LDN 7
IoWrite8(SuperIo_Index_Port, 0x07);
IoWrite8(SuperIo_Data_Port, GPIO_LDN7_DEVICE);

//c. GPIO GP3x(30~37) Input Pin
IoWrite8(SuperIo_Index_Port, GPIO_GROUP_3_IO_REGISTER);
IoWrite8(SuperIo_Data_Port, 0xFF); //0xFF GPIO GP3x(30~37) Input Pin

//d. GPIO Group 3 GP33
UINT8 BitOffset = 3;
UINT8 Data8
IoWrite8(SuperIo_Index_Port, GPIO_GROUP_3_DATA_REGISTER);
Data8 = IoRead8(SuperIo_Data_Port);
Data8 = Data8 >> BitOffset;
Data8 = Data8 & 0x1;
if (Data8){
return 1;// GPIO
```

```
}else{
  return 0;//       GPIO
}

//e.       GPIO GP3x(30~37)    Output Pin
IoWrite8(SuperIo_Index_Port, GPIO_GROUP_3_IO_REGISTER);
IoWrite8(SuperIo_Data_Port, 0x00); //0x00       GPIO GP3x(30~37)              Output Pin

//f.     GPIO Group 3                    GPO                GPIO                GPI
for(GpioNumber=0x30; GpioNumber <= 0x37; GpioNumber++)
{
BitOffset = GpioNumber - 0x30;
IoWrite8(SuperIo_Index_Port, GPIO_GROUP_3_DATA_REGISTER);
Data8 = IoRead8(SuperIo_Data_Port);
Data8 &=~(0x1 << BitOffset);//       bit       0          GPIO
//Data8 |= (0x1 << BitOffset); /*       bit          1          GPIO                */
IoWrite8(SuperIo_Data_Port, Data8);//
}
//g.        Super IO    Configuration Mode
 IoWrite8(SuperIo_Index_Port, 0xAA); //       Super IO Configuration Mode       SuperIO
                          ,                  Configuration Mode
```

8.2 WDT

```
//e.      WDT                5   /
IoWrite8(SuperIo_Index_Port, 0xF1);
IoWrite8(SuperIo_Data_Port, 0x5);

//f.      Super IO   Configuration Mode
IoWrite8(SuperIo_Index_Port, 0xAA);

//      Super IO Configuration Mode      SuperIO                    ,
Configuration Mode
```

9

9.1
